Notice of Allowability	Application No.	Applicant(s)	
	10/623,230	HOWARD ET AL.	
	Examiner	Art Unit	
	Theresa T Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *07/12/04*.

2. ☒ The allowed claim(s) is/are *1-21*.

3. ☒ The drawings filed on *08 December 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 12/08/03
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. Applicant's election of Group I claims 1-21 in the reply filed on 07/12/04 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. This application is in condition for allowance except for the presence of claims 22-30 non-elected without traverse. Accordingly, claims 22-30 have been cancelled.

Reasons for Allowance

4. Claims 1-21 are allowed.

The following is an examiner's statement of reasons for allowance:

The prior art of record fails to disclose the combination of an electronic device recited in the base claims 1, 14 and 21. Specifically, the combination of the structure comprising a buried layer near the top surface, doped with dopant of a first polarity,

electrically communicable to a drain terminal; a body region, having a second top surface, a second bottom surface and a second side surface; a portion of the body region, having doped with dopant of a second polarity, contacting a gate region communicable to a gate terminal; a substantially uniformly doped channel region in the body region, having a third top surface, a third bottom surface, and a third side surface communicable to the portion of the body region, the third bottom surface being substantially coplanar to the second bottom surfaces and contacting the buried layer, the third top surface being substantially coplanar to the second top surface and contacting a source region; and the source region, projecting upward from the channel region, electrically communicable to a source terminal (claim 1); or the combination of an n-channel silicon JFET comprising a buried layer of mono-crystalline silicon near the top surface, doped with a n-type dopant to a sheet resistance of about 25 ohms per square, the buried layer being electrically communicable to a drain terminal near the top surface of the substrate; a silicon mono-crystalline first region having a top surface, a bottom surface and a side surface, the distance between the top and the bottom surfaces being about 0.7 micrometers, the lower portion of the side surface contacting a silicon dioxide region and the upper portion of the side surface contacting a p-type, poly-crystalline silicon gate region, a portion of the first region is p-type; the silicon gate region being communicable to a gate terminal near the top surface of the substrate; a substantially uniformly doped, n-type channel-region in the first region, having a top surface, a bottom surface, and a side surface, the top surface being substantially coplanar to the top surface of the first region, the bottom surface being substantially

coplanar to the bottom surfaces of the first region and electrically communicable to the buried layer, the side surface contacting the p-type portion of the first region; a first n-type, poly-crystalline-silicon-source region, projecting upward from the channel region and the gate region, having a top surface electrically communicable to a source terminal near the top surface of the substrate, a bottom surface electrically communicable to the top surface of the channel region, a side surface in contact with dielectric sidewall spacers; the first n-type, poly-crystalline-silicon-source region that being electrically insulated from the first p-type, poly-crystalline-silicon-gate region; the device being operable channeling an electrical current through the channel region upon a voltage bias being applied between the source terminal and the drain terminal; and the electrical current flowing in a direction substantially perpendicular the top surface of the silicon substrate, the magnitude of the electrical current being a function of a voltage at the gate terminal (claims 14 and 21).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Thursday from 8:00AM - 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TD
September 29, 2004.

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PHAT X. [illegible]
PRIMARY EXAMINER